## REMARKS

These remarks are in response to the Office Action dated June 4, 2010, which has a shortened statutory period for response set to expire September 7, 2010 (September 4-5, 2010 being a Saturday and Sunday and September 6, 2010 being a Federal Holiday). No extension of time is required.

### Claims

Claims 45-62 and 77-85 are pending in the above-identified application. Claims 45-62 and 77-85 are rejected over prior art. Claims 77, 84 and 85 are amended, and Claims 1-44 and 63-76 were previously canceled. Claims 45-62 and 78-83 remain as previously presented. Reconsideration is requested.

### Rejections Under 35 U.S.C. § 103

#### Claims 45, 54-62, 77-78, and 83-85:

Claims 45, 54-62, 77-78, and 83-85 are rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 4,292,668 (Miller et al.) in view of "Design and Characterization of a CMOS Off-Chip Driver/Receiver with Reduced Power-Supply Disturbance" by Hanafi, Hussein I. et al. (Hanafi et al.). The Examiner writes (in part):

> Referring to claim 45, Miller has taught a microprocessor system, comprising:
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> …
>
> g. an oscillator, operating in conjunction with a clock multiplier (Miller column 24, line 35 to column 26, line 35);
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> …
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> Miller has not explicitly taught the oscillator is a CMOS oscillator. However, Miller has taught the oscillator drives the internal clock (Miller column 24, line 35 to column 26, line 35). Hanafi has taught a CMOS signal driver (Hanafi Abstract). A person of ordinary skill in the art at the time the invention was made would have recognized that the CMOS signal driver reduces signal noise without delaying the signal (Hanafi Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate Hanafi's CMOS signal driver into the device of Miller to reduce signal noise without delaying the signal.

Applicants respectfully traverse.

***Principles of Law:***

M.P.E.P. § 2142 provides that the examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not provide a prima facie case of obviousness, then the rejection is improper, and the applicant is under no obligation to submit evidence of non-obviousness.

In *In re Wada and Murphy*, Appeal 2007-3733, Decision on Appeal dated January 14, 2008, pages 7 and 8, the BPAI expressly indicated that, to establish a prima facie case of obviousness, the cited prior art must teach or suggest all the limitations of the claimed invention:

> When determining whether a claim is obvious, an examiner must make "a searching comparison of the claimed invention – *including all its limitations* – with the teaching of the prior art." *In re Ochiai*, 71 F.3d 1565, 1572 (Fed. Cir. 1995) (emphasis added). Thus, "obviousness requires a suggestion of all limitations in a claim." *CFMT, Inc. v. Yieldup Intern. Corp.*, 349 F.3d 1333, 1342 (Fed. Cir. 2003) (citing *In re Royka*, 490 F.2d 981, 985 (CCPA 1974)). Moreover, as the Supreme Court recently stated, "*there must be some articulated reasoning* with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007) (quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (emphasis added)).
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> ...
>
> It is well settled that the "Patent and Trademark Office (PTO) must consider all claim limitations when determining patentability of an invention over the prior art." *In re Lowry*, 32 F.3d 1579, 1582 (Fed. Cir. 1994).
>
> (all emphasis is BPAI's emphasis)

However, a claimed invention composed of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art. *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (2007). Rather, the Examiner must identify a reason that would have prompted a person of ordinary skill in the art to combine the elements in the way the claimed invention does. *Id.* Specifically, as indicated above, there must be some articulated reasoning with a rational underpinning to support a conclusion of obviousness; a

conclusory statement will not suffice. *Id.*, quoting *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

***Argument:***

For the reasons provided in Applicants' prior amendment, Miller et al. does not teach or suggest "a CMOS oscillator, operating in conjunction with a clock multiplier," as recited by Claim 45, because Miller et al. does not indicate that the oscillator 290 (FIG. 14) is a CMOS oscillator.

However, Hanafi et al. also does not teach or suggest "a CMOS oscillator," as recited by Claim 45. Rather, Hanafi et al. discloses a CMOS signal driver and receiver that is "a chip-to-chip signal **interconnection** most suitable for the multichip packaging technology" (*Hanafi et al.*, page 783, §I, last paragraph; emphasis added). It appears from Hanafi et al. that a signal driver is associated with one chip in the multichip system, while the signal receiver is associated with a second chip in the multichip system (*Id.*, Figs. 6-8; page 783, §II; page 785, § III). The driver circuit includes "in" and "out" pins indicating that it receives an input signal from a source on the associated chip and transmits a signal via its output. The signal receiver circuit shown in Fig. 5 also includes input and output pins. The receiver's input receives the signal from the signal driver's output and produces a full-swing voltage output at the second chip in the multichip system (*Id.*, page 785, §III, first paragraph).

Thus, it is clear that the CMOS signal driver/receiver of Hanafi et al. is <u>not</u> "a CMOS oscillator," as recited by Claim 1. Rather, the driver/receiver of Hanafi simply provides a means for connecting two different chips in a multi-chip system. Indeed, neither the signal driver nor signal receiver of Hanafi et al. is a clock.

For the above reasons, because the cited prior art does not teach or suggest all the limitations of Claim 45, no prima facie case of obviousness is established with respect to Claim 45.

Furthermore, Applicants respectfully aver that no prima facie case of obviousness is established with respect to Claim 45, because replacing the oscillator 290 of Miller et al. with the CMOS signal driver and/or signal receiver of Hanafi et al. would render the device of Miller et al. inoperable. Specifically, the CMOS signal driver/receiver of Hanafi et al. is not a clock. Rather, it is a device that provides an interconnection between two chips of a multi-chip system by relaying signals between those chips. Both the driver and the receiver receive and relay provided signals. However, neither appears to provide any sort of signal itself in the absence of a signal that is being communicated between chips. Therefore, replacing the clock 290 of Miller et al. with the signal driver/receiver of Hanafi et al. would result in a circuit that is idle because there would be no clock signal.

For at least these reasons, no prima facie case of obviousness is established with respect to Claim 45. Claims 54-62, 77-78, and 83-85 depend, either directly or indirectly, from Claim 45 and are distinguished, therefore, from the cited prior art for at least the same reasons as Claim 45.

Regarding Claim 77, Claim 77 recites (in part) that "at least said MPU, said IOP, and said MIF are located on-chip" and that "said CMOS oscillator is located off-chip". Hanafi et al. does not teach or suggest that "said CMOS oscillator is located off-chip" because Hanafi et al. does not teach or suggest a CMOS oscillator for the reasons provided above with respect to Claim 45. Furthermore, it appears that the signal driver/receiver of Hanafi et al. is not located off of its respective chip in the multichip system (see e.g., Figs. 6-8 and page 786, §IV, paragraphs 2-3). Rather, Hanafi et al. apparently uses the term "off-chip" to describe the communications between the chips in the multi-chip system and not the physical location of the signal driver/receiver itself. For the above reasons, Claim 77 further distinguishes over the cited prior art. Claim 78 depends from Claim 77 and is, therefore, also further distinguished from the cited prior art for at least the same reasons as Claim 77.

Finally, Claim 77 is amended to add a period at the end of the claim.

Additionally, regarding Claims 45 and 83-85, Applicants note that Claim 45 recites (in part) "a programmable memory interface (MIF)." In the rejection of Claim 45, Miller et al., col. 17, line 30 to col. 18, line 15 and Figure 2 are cited as disclosing the above-recited element of Claim 45. This passage provides the following:

> System bus B distributes power and provides a communications path for data transfers and interrupts between the CPU and each main memory board or I/O controller inserted in bus connectors on the system bus B side of the system. System bus B is similar to system bus A. However, it contains three additional main memory control signals, PMEMGO, PMFRSH, PBSFMD, which are not present on the system bus A. Therefore, main memory boards can only be installed in chassis slots on the system bus B side of the system. All other system bus B signals are similar to the system bus A but are driven by a separate set of drivers. No signals unique to the CPU chassis slot connector are present on system bus B, each signal feeds all chassis slot connectors on system bus B. The operation and control of the system buses A and B are described hereinafter. FIG. 6 gives the functionality and source of each system bus signal.
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> As in the case of system bus A, each I/O controller on system bus B is only allowed to request service (for data transfer or interrupt purposes) at the time that is unique to that IOC and is a function of the position (relative to the CPU) of the IOC on system bus B. Main memory, although located on system bus B, does not make service requests but must still pass on the priority timing signal (BCYCOT-BB and BCYCIN-BB) for use by I/O controllers on system bus B. Although only one I/O controller on a given system bus (A or B) can make a service request at a time, two service requests can be made simultaneously by I/O controllers in the same relative (time slot) position, one on system bus A and one on system bus B. For example, referring to FIG. 2, diskette controller 2, 220-1, on system bus B can make an interrupt request at the same time that printer controller, 208-1, on system bus A makes a DMC data request. **Priority between these simultaneous system bus requests, as well as other outstanding but unresponded to earlier system bus requests, are resolved by the CPU as described hereinafter**.
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> It should be noted that printer controller 208-1 on system bus A is in the second physical bus connector slot, relative to the CPU, and second bus request time slot whereas diskette controller 2, 220-1, is in the fourth physical bus connector slot, relative to the CPU, but in the second bus request time slot on system bus B. The difference between the physical bus connector slot and the bus request time slot on system bus B is due to the fact that each main

> memory board occupies one physical bus connector slot but does not occupy a bus request time slot because main memory never requests the system bus (i.e., main memory does not initiate any data transfers on the system bus and therefore the priority timing signals BCYCOT-BB and BCYCIN-BB need not be delayed by the main memory board).

However, Applicants have reviewed this passage and Figure 2 and cannot determine what is being characterized as a "programmable memory interface" in Miller et al. Figure 2 shows a "memory 1" 214-1, a "memory 2" 216-1, and a "memory save unit" 222. However, none of these elements appear to be a programmable interface.

Furthermore, the above passage is cited as teaching or suggesting that "said MIF is operative to arbitrate and prioritize a plurality of bus transaction requests generated by said MPU and said IOP" as recited by Claim 83. However, the above passage of Miller et al. contradicts this limitation. As indicated above, the CPU of Miller et al., rather than whatever component(s) is/are being characterized as the MIF, resolves priority of the bus requests.

For the above reasons, Claims 45 and 83 further distinguish over the cited prior art. Claims 84-85 inadvertently depended from Claim 82 rather than Claim 83. Therefore, Claims 84-85 are amended to now depend from Claim 83 and are, therefore, further distinguished from the cited prior art for the same additional reasons as Claim 83.

Claims 46-53 and 79-82:

Claims 46-47 and 79-80 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller et al. and Hanafi et al. and further in view of U.S. Patent No. 4,321,706 (Craft). Claims 48-50 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller et al. and Hanafi et al. and further in view of Official Notice. Claims 51-52 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller et al. and Hanafi et al. and further in view of U.S. Patent No. 5,070,451 (Moore et al.). Claim 53 is rejected under 35 U.S.C. § 103 as being unpatentable over Miller et al. and Hanafi et al. and further in view of Official Notice. Claims 81-82 are rejected under 35 U.S.C. § 103 as being unpatentable over Miller et al. and Hanafi et al. and further in view of U.S. Patent No. 5,430,851 (Hirata et al.).

Applicants respectfully traverse.

Each of Claims 46-53 and 79-82 depends, either directly or indirectly, from Claim 45 and, therefore, includes all the limitations of Claim 45. As indicated above, Claim 45 distinguishes over the primary references Miller et al. and Hanafi et al. Furthermore, it does not appear that any of the other cited references teach or suggest the limitations of Claim 45 not taught or suggested by Miller et al. and Hanafi et al. Therefore, each of Claims 46-53 and 79-82 distinguishes over the cited prior art for at least the same reasons as Claim 45. Finally, regarding Claims 48-50 and 53, Applicants respectfully maintain their prior objections that the taking of Official Notice with respect to these claims is improper under MPEP § 2133.03(A).

For the above reasons, Applicants respectfully request reconsideration and withdrawal of all the rejections under 35 U.S.C. § 103.

Request for Constructive Assistance from the Examiner:

Applicants believe that this application discloses patentable subject matter, that the pending claims are directed to that subject matter, and that the pending claims distinguish over the prior art of record. However, Applicants also recognize that the patentable subject matter of the present application is somewhat challenging to claim in a way that gives Applicants the scope of protection to which they are entitled. Therefore, should the Examiner disagree that the pending claims are allowable, Applicants respectfully request the constructive assistance of the Examiner, pursuant to M.P.E.P § 707.07(j)(II) which provides (in part):

> When an application discloses patentable subject matter and it is apparent from the claims and applicant's arguments that the claims are intended to be directed to such patentable subject matter, but the claims in their present form cannot be allowed because of defects in form or omission of a limitation, the examiner should not stop with a bare objection or rejection of the claims. The examiner's action should be constructive in nature and, when possible, should offer a definite suggestion for correction. Further, an examiner's suggestion of allowable subject matter may justify indicating the possible desirability of an interview to accelerate early agreement on allowable claims.

For the foregoing reasons, Applicants believe that Claims 45-62 and 77-85 are in condition for allowance. Should the Examiner undertake any action other than allowance of Claims 45-62 and 77-85, or if the Examiner has any questions or suggestions for expediting the prosecution of this application, the Examiner is requested to contact Applicants' attorney at (269) 279-8820.

Respectfully submitted,

September 7, 2010 /Larry E. Henneman, Jr./

Date:_____ _____

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**CERTIFICATE OF TRANSMISSION (37 CFR 1.8(a))**

I hereby certify that this paper (along with any referred to as being attached or enclosed) is being electronically filed with the U.S. Patent and Trademark Office on the date shown below.

September 7, 2010 /Larry E. Henneman, Jr./

Date:_____ _____

Larry E. Henneman, Jr.